REMARKS

Applicant respectfully requests reconsideration and allowance of the subject application. Claims 9, 18, 20, 23, 30-33, 42, 57, 60, and 62 are amended. Claim 29 is canceled without prejudice. Claims 1-28 and 30-91 are pending in this application.

Specification

In the March 31 Office Action, at p. 2, it was stated that:

> The arrangement of the disclosed application does not conform with 37 CFR 1.77(b).
>
> Section headings are underlined and boldfaced throughout the disclosed specification. Section headings should not be underlined and/or **boldfaced**. Appropriate corrections are required according to the guidelines provided below

Applicant respectfully submits that the specification does conform with 37 CFR §1.77. The guidelines referenced at pp. 2-3 of the March 31 Office Action are guidelines suggested for use, as acknowledged in the March 31 Office Action at p. 2. These guidelines are not requirements of 37 CFR §1.77, and 37 CFR §1.77 does not require that these suggested guidelines be followed verbatim. Accordingly, Applicant respectfully submits that the specification does conform with 37 CFR §1.77, and that no correction is required.

35 U.S.C. § 112

Claims 9, 18, 20, 31, and 33 stand rejected under 35 U.S.C. §112, second paragraph. As part of this response, claims 9, 18, 20, 31, and 33 have been amended, and Applicant respectfully submits that claims 9, 18, 20, 31, and 33, as amended, comply with 35 U.S.C. §112, second paragraph.

Applicant respectfully requests that the §112 rejections be withdrawn.

35 U.S.C. § 102

Claims 1, 6-7, 12-13, 16, 22-29, 34-39, 43-45, 57-60, 64-66, 68-74, and 79-91 stand rejected under 35 U.S.C. §102(e) as being unpatentable over U.S. Patent No. 6,557,104 to Vu et al. (hereinafter "Vu"). Claim 29 has been canceled without prejudice. Applicant respectfully submits that claims 1, 6-7, 12-13, 16, 22-28, 34-39, 43-45, 57-60, 64-66, 68-74, and 79-91 are not anticipated by Vu.

Vu is directed to a method and apparatus for secure processing of cryptographic keys (see, Title). Vu uses a special secure processing mode to process a cryptographic key provided on a token and an associated special secure memory area which is transparent to the operating system (see, col. 3, lines 61-64). One example of a secure mode is the System Management Mode (SMM) of the Intel x86 processor architecture, and the associated memory is known as System management RAM (SMRAM) (see, col. 3, line 64 – col. 4, line 1). The cryptographic key and algorithms, once stored into SMRAM, can be used during SMM such that both the cryptographic key and its processing are never exposed (see, col. 4, lines 4-7).

In contrast, claim 1 recites, in part:

> allowing operation of the computer to begin based on untrusted code;
>
> loading, under control of the untrusted code, a trusted core into memory;

> preventing each of one or more central processing units and each of one or more bus masters in the computer from accessing the memory;
>
> resetting each of the one or more central processing units;
>
> allowing one central processing unit to access the memory and execute trusted core initialization code to initialize the trusted core; and
>
> after execution of the trusted core has been initialized, allowing any other central processing units and any bus masters in the computer to access the memory.

Applicant respectfully submits that Vu does not disclose these elements of claim 1.

Applicant respectfully submits that Vu does not disclose the resetting each of the one or more central processing units as recited in claim 1. Vu does discuss that the cryptographic key and program may be loaded after the system has already booted, as long as the loading is done in SMM (see, col. 6, lines 6-8). However, there is no discussion or mention in Vu that using SMM involves resetting the processor. In the March 31 Office Action at p. 5, Vu at col. 5 lines 27-35 is cited as teaching the resetting of claim 1. In the cited portion of Vu, Vu discusses that SMM can be entered by invoking a software System Management Interrupt (SMI), and that the processor can exit SMM (see, col. 5, lines 28-30 and 40-41). However, nowhere is there any mention that this entering or exiting SMM involves resetting the processor. Absent any such discussion or mention in Vu, Applicant respectfully submits that Vu cannot disclose the resetting of claim 1.

Furthermore, Applicant respectfully submits that Vu does not disclose preventing each of one or more central processing units and each of one or more bus masters in the computer from accessing the memory, and after execution of the trusted core has been initialized, allowing any other central processing units and any bus masters in the computer to access the memory as recited in claim 1.

From the cited portions of Vu, it appears that the SMRAM of Vu is being relied on as teaching the memory referred to in claim 1. However, Applicant respectfully submits that nowhere does Vu discuss that each of one or more central processing units and each of one or more bus master in the computer are prevented from accessing the SMRAM. Rather, Vu discusses that the SMRAM is locked, which prevents any other processes from accessing the data stored in the SMRAM (see, col. 4, lines 63-65). Thus, Vu is directed to preventing other processes from accessing the SMRAM, not preventing the processor of Vu from accessing the SMRAM. Applicant respectfully submits that nowhere in Vu is there any discussion or mention of preventing the processor of Vu from accessing the SMRAM. In fact, if the processor of Vu were prevented from accessing the SMRAM, it would not be possible for the processor to execute the requested security processing in the SMM discussed in col. 5, lines 24-48 because those programs are stored in the SMRAM (see, col. 5, lines 35-36). Thus, Applicant respectfully submits that Vu cannot disclose preventing each of one or more central processing units and each of one or more bus masters in the computer from accessing the memory as recited in claim 1.

Additionally, Applicant respectfully submits that the SMRAM cannot be used as a basis for disclosing after execution of the trusted core has been initialized, allowing any other central processing units and any bus masters in the computer to access the memory as recited in claim 1. There is no discussion or mention in Vu that the SMRAM can be accessed by any other processor or bus master in the computer system. Absent such a discussion, Applicant respectfully submits that Vu cannot disclose allowing any other central processing units and any bus masters in the computer to access the memory as recited in claim 1.

For at least these reasons, Applicant respectfully submits that claim 1 is allowable over Vu.

Given that claims 6, 7, 12, 13, 16, 22, and 71-74 depend from claim 1, Applicant respectfully submits that claims 6, 7, 12, 13, 16, 22, and 71-74 are likewise allowable over Vu for at least the reasons discussed above with respect to claim 1.

With respect to amended claim 23, Applicant respectfully submits that, similar to the discussion above regarding claim 1, Vu does not disclose resetting each of the one or more central processing units after each of the one or more central processing units has been prevented from accessing the memory and after each of the one or more bus masters has been prevented from accessing the memory as recited in amended claim 23. Furthermore, Applicant respectfully submits that, similar to the discussion above regarding claim 1, Vu does not disclose preventing each of one or more central processing units in the computer from accessing the memory and after execution of the trusted core initialization process, allowing any other central processing units and any of the one or more bus masters to access the memory as recited in amended claim 23.

For at least these reasons, Applicant respectfully submits that amended claim 23 is allowable over Vu.

Given that claims 24-28 and 34-35 depend from amended claim 23, Applicant respectfully submits that claims 24-28 and 34-35 are likewise allowable over Vu for at least the reasons discussed above with respect to amended claim 23.

With respect to claim 36, claim 36 recites:

> A method comprising:
> allowing a computer to begin operation based on untrustworthy code;
> loading, under the control of the untrustworthy code, additional code into memory; and
> initiating execution of the additional code in a secure manner despite the untrustworthy code in the computer.

Applicant respectfully submits that Vu does not disclose loading, under the control of the untrustworthy code, additional code into memory, and initiating execution of the additional code in a secure manner despite the untrustworthy code in the computer as recited in claim 36.

Vu discusses that the cryptographic key and program may be loaded after the system has already booted (see, col. 6, lines 6-7). However, Vu goes on to state that such can occur as long as the loading is done in the SMM (see, col. 6, lines 7-8), and that the loading and processing of the cryptographic keys and programs are performed in the secure processor mode using the secure memory (see, col. 6, lines 17-21). The secure mode and the secure memory area are not visible to the applications previously running on the processor (see, col. 5, lines 44-47). Thus, Vu discusses that the loading is to be done in the secure mode, which is not visible to applications previously running on the processor. If the secure mode and the secure memory area are not visible to applications previously running on the processor, then Applicant respectfully submits that those applications cannot control loading of additional code into memory, and thus cannot disclose loading, under the control of the untrustworthy code, additional code into memory as recited in claim 36.

For at least these reasons, Applicant respectfully submits that claim 36 is allowable over Vu.

With respect to claim 38, claim 38 depends from claim 36 and Applicant respectfully submits that claim 38 is allowable over Vu for at least the reasons discussed above with respect to claim 36. Furthermore, Applicant respectfully submits that, similar to the discussion above regarding claim 1, Vu does not disclose resetting each of the one or more central processing units as recited in claim 38. Additionally, Applicant respectfully submits that, similar to the discussion above regarding claim 1, Vu does not disclose preventing each of one or more central processing units in the computer from accessing the memory, preventing each of one or more bus masters in the computer from accessing the memory, and after execution of the code initialization process, allowing any other central processing units and any of the one or more bus masters to access the memory as recited in claim 38.

For at least these reasons, Applicant respectfully submits that claim 38 is allowable over Vu.

With respect to claim 43, claim 43 depends from claim 36 and Applicant respectfully submits that claim 43 is allowable over Vu for at least the reasons discussed above with respect to claim 36. Furthermore, claim 43 recites, in part:

> receiving, from a central processing unit, a read request corresponding to a central processing unit reset vector;
>
> responding to the read request with instructions to cause the central processing unit to jump to a starting location of the trusted core.

Applicant respectfully submits that there is no discussion or mention in Vu of a central processing unit reset vector, much less of the receiving and responding of claim 43.

In the March 31 Office Action at p. 10, Vu at col. 5, lines 27-36 is cited as disclosing the receiving and responding of claim 43. Applicant respectfully disagrees with this characterization of Vu. The cited portion of Vu discusses invoking a software System Management Interrupt (SMI), accessing the cryptographic key and programs stored in the SMRAM, and performing the requested security processing in the SMM. Nowhere in this cited portion is there any discussion or mention of receiving, from a central processing unit, a read request corresponding to a central processing unit reset vector as recited in claim 43 – there is no mention whatsoever of a central processing unit reset vector in the cited portion (or elsewhere) of Vu. Furthermore, nowhere in this cited portion of Vu is there any discussion or mention of responding to the read request with instructions to cause the central processing unit to jump to a starting location of the trusted core. Applicant respectfully submits that the mere discussion of SMM and invoking a software System Management Interrupt does not disclose responding to the read request with instructions to cause the central processing unit to jump to a starting location of the trusted core as recited in claim 43.

For at least these reasons, Applicant respectfully submits that claim 43 is allowable over Vu.

Given that claims 37, 39, 44, and 45 depend from claim 36, Applicant respectfully submits that claims 37, 39, 44, and 45 are likewise allowable over Vu for at least the reasons discussed above with respect to claim 36.

With respect to amended claim 57, amended claim 57 recites:

> An apparatus comprising:
>
> a processor reset portion to assert a reset signal to a processor; and
>
> a memory protector portion to prevent any bus master from accessing memory until the processor completes execution of a trusted core initialization process, and to allow any bus master to access the memory after the processor completes execution of the trusted core initialization process.

Applicant respectfully submits that Vu does not disclose a memory protector portion as recited in amended claim 57.

Applicant respectfully submits that there is no disclosure in Vu of a memory protector portion to prevent any bus master from accessing memory until the processor completes execution of a trusted core initialization process, and to allow any bus master to access the memory after the processor completes execution of the trusted core initialization process. Vu discusses that the SMRAM is locked, which prevents any other processes from accessing the data stored in the SMRAM (see, col. 4, lines 63-65). Vu further discusses that the SMRAM is locked and hidden by the chipset before the operating system is loaded, making the SMRAM's contents tamper-proof from the operating system (see, col. 5, lines 4-7). However, there is no discussion or mention in Vu of allowing any bus master to access the SMRAM of Vu. As such, Applicant respectfully submits that there cannot be any disclosure in Vu of a memory protection portion to allow any bus master to access the memory after the processor completes execution of the trusted core initialization process as recited in amended claim 57, much less of the memory protection portion also to prevent any bus master from accessing memory until the processor completes execution of a trusted core initialization process as recited in amended claim 57.

For at least these reasons, Applicant respectfully submits that amended claim 57 is allowable over Vu.

Given that claims 58-60, 64-65, and 79-82 depend from amended claim 57, Applicant respectfully submits that claims 58-60, 64-65, and 79-82 are likewise allowable over Vu for at least the reasons discussed above with respect to amended claim 57.

With respect to claim 66, Applicant respectfully submits that, similar to the discussion above regarding amended claim 57, Vu does not disclose a memory controller being configured to prevent the bus master from accessing the system memory until after the trusted core initialization process is completed as recited in claim 66. For at least these reasons, Applicant respectfully submits that claim 66 is allowable over Vu.

Given that claims 83-87 depend from claim 66, Applicant respectfully submits that claims 83-87 are likewise allowable over Vu for at least the reasons discussed above with respect to claim 66.

With respect to claim 68, claim 68 recites:

> A method comprising:
> allowing execution of different trusted cores in a computer to be initiated serially without requiring the computer to be re-booted.

Applicant respectfully submits that Vu does not disclose allowing execution of different trusted cores in a computer to be initiated serially without requiring the computer to be re-booted as recited in claim 68.

Vu discusses that when an application program needs to access a secure computer system or network, it invokes the Security Services routine of Vu, which in turn invokes a software System Management Interrupt (SMI) (see, col. 5, lines 24-30). The SMI initializes the system processor into SMM, and a software SMI handler invokes the security function (see, col. 5, lines 30-35). The security function then accesses the cryptographic key and programs stored in the SMRAM (see, col. 5, lines 35-36).

However, there is no discussion or mention in Vu that execution of different security functions or different cryptographic programs is initiated serially. Nowhere in Vu is there any discussion or mention that when an application program needs to access a secure computer system or network, that execution of different security functions or different cryptographic programs is initiated serially. Rather, Vu discusses only a single security function accessing the same cryptographic programs. As such, Applicant respectfully submits that Vu cannot disclose allowing execution of different trusted cores in a computer to be initiated serially without requiring the computer to be re-booted as recited in claim 68.

For at least these reasons, Applicant respectfully submits that claim 68 is allowable over Vu.

Given that claims 69-70 depend from claim 68, Applicant respectfully submits that claims 69-70 are likewise allowable over Vu for at least the reasons discussed above with respect to claim 68.

With respect to claim 88, Applicant respectfully submits that, similar to the discussion above regarding claim 1, Vu does not disclose preventing each of one or more central processing units and each of one or more bus masters in the computer from accessing the memory, and after execution of the trusted core has been initialized, allowing any other central processing units and any bus masters in the computer to access the memory as recited in claim 88. Furthermore, Applicant respectfully submits that, similar to the discussion above regarding claim 36, Vu does not disclose loading, under control of the untrusted code, a trusted core into memory of the computer as recited in claim 88.

For at least these reasons, Applicant respectfully submits that claim 88 is allowable over Vu.

Given that claims 89-91 depend from claim 88, Applicant respectfully submits that claims 89-91 are likewise allowable over Vu for at least the reasons discussed above with respect to claim 88.

Claims 46, 48-52, and 75-78 stand rejected under 35 U.S.C. §102(b) as being unpatentable over U.S. Patent No. 5,778,070 to Mattison (hereinafter "Mattison '070"). Applicant respectfully submits that claims 46, 48-52, and 75-78 are not anticipated by Mattison'070.

With respect to claim 46, claim 46 recites:

> A memory controller comprising:
> a first interface to allow communication with a processor;
> a second interface to allow communication with a system memory; and
> a controller, coupled to the first interface and the second interface, to reset a processor and to allow the processor to execute a code initialization process while preventing any other processors from accessing the system memory.

Applicant respectfully submits that Mattison '070 does not disclose a controller to reset a processor and to allow the processor to execute a code initialization process while preventing any other processors from accessing the system memory as recited in claim 46.

Mattison '070 is directed to a method and apparatus for protecting flash memory (see, Title). In Mattison '070, flash memory is reprogrammed by first loading a flash memory upgrade program containing a new flash memory image into system memory and executing the flash memory upgrade program (see, col. 7, line 64 – col. 8, line 2). After the flash memory upgrade program begins execution, the flash memory upgrade program calls a special function in the current program contained in flash memory, requesting to install the new flash memory image (see, col. 8, lines 9-13). After the processor begins operating according to the current program contained in flash memory, a memory address/window detector disables caching by the processor and the memory controller (see, col. 8, lines 28-32). The current program in flash memory would then verify the source and content of the flash memory upgrade program (see, col. 9, lines 38-41), and enable reprogramming of the flash memory (see, col. 98, lines 59-61). The flash memory upgrade program erases the flash memory and copies the new flash memory image into the flash memory (see, col. 10, lines 9-12), then transfers control of the processor to the program contained in the new flash memory image, now in the flash memory (see, col. 10, lines 15-18).

However, Applicant respectfully submits that Mattison '070 does not disclose a memory controller comprising a controller to reset a processor as recited in claim 46. In the March 31 Office Action at p. 17, Mattison '070 at col. 8, lines 29-38 is cited as teaching a memory controller comprising a controller to reset a processor. Applicant respectfully disagrees with this characterization of Mattison

‘070. The cited portion of Mattison ‘070 discusses disabling caching by the processor 102 and the memory controller 104 of Mattison ’070. There is no discussion or mention in the cited portion of Mattison ‘070, or elsewhere in Mattison ‘070, of the memory controller of Mattison ‘070 comprising a controller to reset a processor. As such, Applicant respectfully submits that Mattison ‘070 cannot disclose a memory controller comprising a controller to reset a processor as recited in claim 46.

For at least these reasons, Applicant respectfully submits that claim 46 is allowable over Mattison ‘070.

Given that claims 48-52, and 75-78 depend from claim 46, Applicant respectfully submits that claims 48-52, and 75-78 are likewise allowable over Mattison ‘070 for at least the reasons discussed above with respect to claim 46.

Applicant respectfully requests that the §102 rejections be withdrawn.

35 U.S.C. § 103

Claims 2-4, 17-21, 30-33, 40-42, and 62-63 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Vu in view of U.S. Patent No. 6,480,948 to Virajpet et al. (hereinafter “Virajpet”). Applicant respectfully submits that claims 2-4, 17-21, 30-33, 40-42, and 62-63 are not obvious over Vu in view of Virajpet.

With respect to claim 2, claim 2 depends from claim 1 and Applicant respectfully submits that claim 2 is not obvious over Vu for at least the reasons discussed above with respect to claim 1. Furthermore, Applicant respectfully submits that Virajpet is not cited as curing, and does not cure, the deficiencies of

Vu discussed above with respect to claim 1. For at least these reasons, Applicant respectfully submits that claim 2 is allowable over Vu in view of Virajpet.

Given that claims 3-4 depend from claim 2, Applicant respectfully submits that claims 3-4 are likewise allowable over Vu in view of Virajpet for at least the reasons discussed above with respect to claim 2.

With respect to claim 17, claim 17 depends from claim 1 and Applicant respectfully submits that claim 17 is not obvious over Vu for at least the reasons discussed above with respect to claim 1. Furthermore, Applicant respectfully submits that Virajpet is not cited as curing, and does not cure, the deficiencies of Vu discussed above with respect to claim 1.

Furthermore, in the March 31 Office Action at p. 21, Vu at col. 5, lines 27-40 is cited as disclosing the receiving, returning, and allowing of claim 17. Applicant respectfully disagrees with this characterization of Vu. The cited portion of Vu discusses invoking a software System Management Interrupt (SMI), accessing the cryptographic key and programs stored in the SMRAM, and performing the requested security processing in the SMM. Nowhere in this cited portion is there any discussion or mention of receiving, from a central processing unit, a read request corresponding to a central processing unit reset vector as recited in claim 17 – there is no mention whatsoever of a central processing unit reset vector in the cited portion (or elsewhere) of Vu. Furthermore, nowhere in this cited portion of Vu is there any discussion or mention of responding to the read request with instructions to cause the central processing unit to jump to a starting location of the trusted core. Applicant respectfully submits that the mere discussion of SMM and invoking a software System Management Interrupt does not disclose responding to the read request with instructions to cause the central processing unit to jump to a starting location of the trusted core as recited in claim 17.

With respect to Virajpet, Applicant respectfully submits that there is no discussion in Virajpet of mapping a central processing unit reset vector to an initialization vector, much less of returning, in response to the read request, the initialization vector to the one central processing unit as recited in claim 17.

Virajpet discusses two memory maps for a computer system (see, col. 3, lines 1-2). The first memory map is used during a first time period, after reset, directing memory accesses to an internal ROM and/or external ROM (see, col. 3, lines 8-17). The second memory map is used during a second time period, after all preliminary operations associated with the reset condition are completed, directing memory accesses to a relatively fast internal RAM (see, col. 3, lines 18-28). This allows access for interrupt vectors or interrupt code to be to a relatively fast SRAM device rather than a relatively slower non-volatile memory device (see, col. 3, lines 24-27).

However, in Virajpet, the address 00000000 (hex) is the reset address (see, col. 1, lines 27-32 and 39-41). There is no discussion in Virajpet of this address being mapped. Virajpet, as discussed above, is directed to mapping interrupt vectors or interrupt code so that they can be accessed using a faster RAM device rather than a relatively slower non-volatile memory device. Access to the 00000000 (hex) reset address of Virajpet, however, are to the slower ROM (see, col. 3, line 64 – col. 4, line 7). Without any mention of accessing the 00000000 (hex) reset address of Virajpet from anything other than the slower ROM, Applicant respectfully submits that Virajpet cannot disclose or suggest mapping a central processing unit reset vector to an initialization vector, much less returning, in response to the read request, the initialization vector to the one central processing unit as recited in claim 17.

For at least these reasons, Applicant respectfully submits that claim 17 is allowable over Vu in view of Virajpet.

Given that claims 18-21 depend from claim 17, Applicant respectfully submits that claims 18-21 are likewise allowable over Vu in view of Virajpet for at least the reasons discussed above with respect to claim 17.

With respect to claim 30, Applicant respectfully submits that, similar to the discussion above regarding claim 17, Virajpet does not disclose or suggest mapping a central processing unit reset vector to an initialization vector, much less returning, in response to the read request, the initialization vector to the one central processing unit as recited in claim 30. Additionally, Vu is not cited as disclosing or suggesting, and does not disclose or suggest, such mapping and returning.

For at least these reasons, Applicant respectfully submits that claim 30 is allowable over Vu in view of Virajpet.

Given that claims 31-33 depend from claim 30, Applicant respectfully submits that claims 31-33 are likewise allowable over Vu in view of Virajpet for at least the reasons discussed above with respect to claim 30.

With respect to claim 40, claim 40 depends from claim 36 and Applicant respectfully submits that claim 40 is not obvious over Vu for at least the reasons discussed above with respect to claim 36. Furthermore, Applicant respectfully submits that Virajpet is not cited as curing, and does not cure, the deficiencies of Vu discussed above with respect to claim 36. In addition, Applicant respectfully submits that, similar to the discussion above regarding claim 17, Virajpet does not disclose or suggest mapping a central processing unit reset vector to an initialization vector, much less returning, in response to the read request, the initialization vector to the one central processing unit as recited in claim 40.

For at least these reasons, Applicant respectfully submits that claim 40 is allowable over Vu in view of Virajpet.

Given that claim 41 depends from claim 40, Applicant respectfully submits that claim 41 is likewise allowable over Vu in view of Virajpet for at least the reasons discussed above with respect to claim 40.

With respect to claim 42, claim 42 depends from claim 36 and Applicant respectfully submits that claim 42 is not obvious over Vu for at least the reasons discussed above with respect to claim 36. Furthermore, Applicant respectfully submits that Virajpet is not cited as curing, and does not cure, the deficiencies of Vu discussed above with respect to claim 36.

In addition, Applicant respectfully submits that Vu in view of Virajpet does not disclose or suggest remapping the additional code to appear at an address where a central processing unit starts executing after being reset, the additional code having been loaded under the control of the untrustworthy code as recited in claim 42. As discussed above, Vu stores the cryptographic key and algorithms in the System Management RAM (SMRAM). There is no discussion or mention in either Vu or Virajpet of why such cryptographic key and algorithms would need to be mapped to some other memory. The cryptographic key and algorithms could not be mapped out of the SMRAM of Vu because they would need to remain in the SMRAM in order to maintain the secure processing discussed in Vu. Thus, Applicant respectfully submits that Vu in view of Virajpet cannot disclose or suggest remapping the additional code to appear at an address where a central processing unit starts executing after being reset, the additional code having been loaded under the control of the untrustworthy code as recited in claim 42.

For at least these reasons, Applicant respectfully submits that claim 42 is allowable over Vu in view of Virajpet.

With respect to claim 62, Applicant respectfully submits that, similar to the discussion above regarding claim 17, Virajpet does not disclose or suggest a controller to map a processor reset vector to an initialization vector, much less to return, in response to the read request, the initialization vector to the processor as recited in claim 62. Additionally, Vu is not cited as disclosing or suggesting, and does not disclose or suggest, such a controller.

For at least these reasons, Applicant respectfully submits that claim 62 is allowable over Vu in view of Virajpet.

Given that claim 63 depends from claim 62, Applicant respectfully submits that claim 63 is likewise allowable over Vu in view of Virajpet for at least the reasons discussed above with respect to claim 62.

Claims 5 and 10 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Vu in view of U.S. Patent No. 6,546,489 to Frank, Jr. et al. (hereinafter "Frank"). Applicant respectfully submits that claims 5 and 10 are not obvious over Vu in view of Frank.

Claims 5 and 10 depend from claim 1 and Applicant respectfully submits that claims 5 and 10 are not obvious over Vu for at least the reasons discussed above with respect to claim 1. Furthermore, Applicant respectfully submits that Frank is not cited as curing, and does not cure, the deficiencies of Vu discussed above with respect to claim 1. For at least these reasons, Applicant respectfully submits that claims 5 and 10 are allowable over Vu in view of Frank.

Claims 8-9 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Vu in view of U.S. Patent No. 6,477,252 to Faber et al. (hereinafter "Faber"). Applicant respectfully submits that claims 8-9 are not obvious over Vu in view of Faber.

Claims 8-9 depend from claim 1 and Applicant respectfully submits that claims 8-9 are not obvious over Vu for at least the reasons discussed above with respect to claim 1. Furthermore, Applicant respectfully submits that Faber is not cited as curing, and does not cure, the deficiencies of Vu discussed above with respect to claim 1. For at least these reasons, Applicant respectfully submits that claims 8-9 are allowable over Vu in view of Faber.

Claim 11 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Vu in view of U.S. Patent No. 5,349,643 to Cox et al. (hereinafter "Cox"). Applicant respectfully submits that claim 11 is not obvious over Vu in view of Cox.

Claim 11 depends from claim 1 and Applicant respectfully submits that claim 11 is not obvious over Vu for at least the reasons discussed above with respect to claim 1. Furthermore, Applicant respectfully submits that Cox is not cited as curing, and does not cure, the deficiencies of Vu discussed above with respect to claim 1. For at least these reasons, Applicant respectfully submits that claim 11 is allowable over Vu in view of Cox.

Claims 14-15 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Vu in view of U.S. Patent No. 6,378,072 to Collins et al. (hereinafter "Collins"). Applicant respectfully submits that claims 14-15 are not obvious over Vu in view of Collins.

Claims 14-15 depend from claim 1 and Applicant respectfully submits that claims 14-15 are not obvious over Vu for at least the reasons discussed above with respect to claim 1. Furthermore, Applicant respectfully submits that Collins is not cited as curing, and does not cure, the deficiencies of Vu discussed above with respect to claim 1. For at least these reasons, Applicant respectfully submits that claims 14-15 are allowable over Vu in view of Collins.

Claim 47 stands rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,615,355 to Mattison (hereinafter "Mattison '355") in view of "486 Microprocessors", SSV Software Systems (hereinafter "486 Microprocessors reference"). Applicant respectfully submits that claim 47 is not obvious over Mattison '355 in view of the 486 Microprocessors reference.

Claim 47 depends from claim 46 and Applicant respectfully submits that claim 47 is not obvious over Mattison '070 (as well as Mattison '355, which is a continuation of Mattison '070) for at least the reasons discussed above with respect to claim 46. Furthermore, Applicant respectfully submits that the 486 Microprocessors reference is not cited as curing, and does not cure, the deficiencies of Mattison '070 (and thus Mattison '355) discussed above with respect to claim 46. For at least these reasons, Applicant respectfully submits that claim 47 is allowable over Mattison '355 in view of the 486 Microprocessors reference.

Claims 53-56 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Mattison '355 in view of Virajpet and further in view of Vu. Applicant respectfully submits that claims 53-56 are not obvious over Mattison '355 in view of Virajpet and Vu.

Claim 53 depends from claim 46 and Applicant respectfully submits that claim 53 is not obvious over Mattison '070 (as well as Mattison '355, which is a continuation of Mattison '070) for at least the reasons discussed above with respect to claim 46. Furthermore, Applicant respectfully submits that Virajpet and Vu are not cited as curing, and do not cure, the deficiencies of Mattison '070 (and thus Mattison '355) discussed above with respect to claim 46.

Furthermore, Applicant respectfully submits that, similar to the discussion above regarding claim 17 and contrary to the assertion in the March 31 Office Action at p. 34 regarding Virajpet and Vu, Virajpet and Vu do not disclose or suggest a controller to map a processor reset vector to an initialization vector, much less to return, in response to the read request, the initialization vector to the processor as recited in claim 53. Mattison '355 is not cited as curing, and does not cure, these deficiencies of Virajpet and Vu.

For at least these reasons, Applicant respectfully submits that claim 53 is allowable over Mattison '355 in view of Virajpet and Vu.

Given that claims 54-56 depend from claim 53, Applicant respectfully submits that claims 54-56 are likewise allowable over Mattison '355 in view of Virajpet and Vu for at least the reasons discussed above with respect to claim 53.

Claims 61 and 67 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Vu in view of U.S. Patent No. 5,175,829 to Stumpf et al. (hereinafter "Stumpf"). Applicant respectfully submits that claims 61 and 67 are not obvious over Vu in view of Stumpf.

Claim 61 depends from claim 57 and Applicant respectfully submits that claim 61 is not obvious over Vu for at least the reasons discussed above with respect to claim 57. Furthermore, Applicant respectfully submits that Stumpf is not cited as curing, and does not cure, the deficiencies of Vu discussed above with respect to claim 57. For at least these reasons, Applicant respectfully submits that claim 61 is allowable over Vu in view of Stumpf.

Claim 67 depends from claim 66 and Applicant respectfully submits that claim 67 is not obvious over Vu for at least the reasons discussed above with respect to claim 66. Furthermore, Applicant respectfully submits that Stumpf is not cited as curing, and does not cure, the deficiencies of Vu discussed above with respect to claim 66. For at least these reasons, Applicant respectfully submits that claim 67 is allowable over Vu in view of Stumpf.

Applicant respectfully requests that the §103 rejections be withdrawn.

Conclusion

Claims 1-28 and 30-91 are in condition for allowance. Applicant respectfully requests reconsideration and issuance of the subject application. Should any matter in this case remain unresolved, the undersigned attorney respectfully requests a telephone conference with the Examiner to resolve any such outstanding matter.

Respectfully Submitted,

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